Int. J. Adv. Res. Sci. Technol. Volume 5, Issue 2, 2016, pp.610-616.

IJARST

International Journal of Advanced Research in Science and Technology

journal homepage: www.ijarst.com

ISSN 2319 – 1783 (Print)

ISSN 2320 – 1126 (Online)

A Review on Semiconductor Fabrication to FPGA.

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ARTICLEINFO

Article history:

Received :23 July 2016

Accepted :27 Sep. 2016

Available online :10 Oct. 2016

Keywords:

ASIC,

FPGA,

DSP,

RAM.

ABSTRACT

Researchers are experimenting with carbon nanotubes to Phenomenally change the way semiconductor devices are made. At the same time, there are innovations to address immediate needs such as improving yield, decreasing time – to – market, reducing leakage power, thermal management in multi – die stacks, new layout requirement and so on.

The 'Chips' are everywhere today, right from mobile phones and computer to microwave ovens and washing machines, and even in children's toys. There are millions of chips in the world and more are being produced every day, but did you know that these are still produced by a countable number of manufacturers across manufacturing plant, is a technology and resource – intensive factory that could cost anywhere between 1 billion and 10 billion dollars, or even more to set up.

PAPER-QR CODE

IJARST

Volume 5, Issue 2

Citation: *J Mahesh Kumar, A Review on Semiconductor Fabrication by FPGA, Int. J. Adv. Res. Sci. Technol. Volume 5, Issue 2, 2016, pp.610-616.*

1. FPGAs Not Just Logic Gates Any More! More than ASIC'S:

While the debate on ASIC versus FPGA continues, today's FPGAs with integrated functional blocks like high – speed transceivers DSP blocks, hard IPs like PCI express and Ethernet MAC, and DDR3 memory controllers have surpassed ASIC in many embedded applications. These have now become designers' choice in communication, defiance, medical, consumer electronics and many more devices.

1.1 Introduction:

The challenges and resulting improvements in semiconductor fabrication technology can be attributed to the complexity and sensitivity of the whole process. It could take six to eight weeks per batch right from wafer processing and die preparation to integrated circuit packaging and testing. What's more, it is a very sensitive process too. As chips get smaller, purer materials are sought. The 'clean rooms' of fabs, where most of the processes happen, need to be cleaner than you can imagine. Human workers need to wear special suits so that chips do not get contaminated. High – precision machines are needed because working is required at the micrometer and nanometer scale with very sensitive materials.

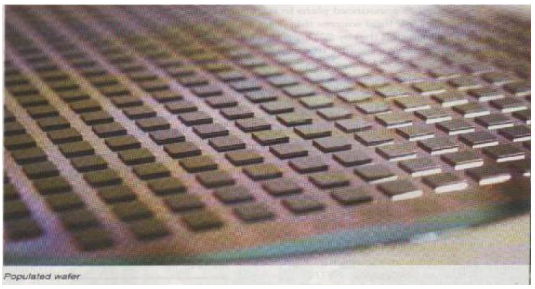

Figure: 1. Three dimensional integrated circuits (3D ICs)

As the industry transitioned from micro – to nanometer scales, the onus was on the fabs to execute the engineer's dreams, and they did. Now even 40nm technologies have entered the mainstream and smaller feature sizes are on the anvil. Technologies such as three dimensional integrated circuits (3D ICs) are promising a dramatic reduction in the size of chips in

this decade, while research in the field of carbon nanotubes is indicating the arrival of a revolution as innovations continue to fire our dreams.

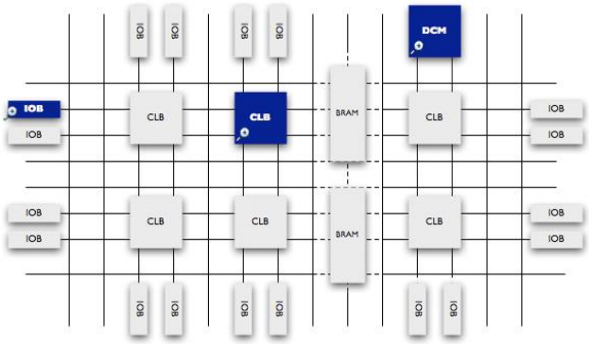

Figure: 2. FPGA block structure

1.2 FPGA block structure:

Earlier, if we were to summaries the ASIC versus FPGA battle for cost and performance, ASICs had a greater penetration because there was demand for high – volume applications in which application – specific integrated circuits (ASICs) provided a cost effective solution and field – programmable gate arrays (FPGAs) were a costlier affair. However, now we see a reversal in trend. Experts say that the cost of entry for ASIC design in skyrocketing, which has made FPGAs a natural choice. A Part from the cost, the reduced time – to – market and design flexibility have made FPGAs relevant for more and more embedded applications.

Traditionally, ASICs were preferred in high – voltage applications because of the overall low cost of production. "Today, the demand for ultra – high – volume products is reducing and so is demand for ASICs," "Last year use of ASICs declined by 21 percent for the simple reason of exorbitant cost associated with them." Market segments like communication (routers, switches, back – haul equipment, and wireless pico and femto cells) and high – end consumer electronics (flat – Panel plasma TVs) centre around FPGAs. Medical, Industrial, defense, security and surveillance related applications are also designed using FPGAs.

"Use of FPGAs offers great flexibility, scalability / reprogram ability and almost zero non – recurring engineering (NRE) cost" explains Apurva Prabhakar, senior design engineer, embedded group, Kritikal Solutions. She adds, "For designing with FPGAs, you have easy-to-use and less complex design tools. For simple designs, a single integrated tool for simulation, synthesis, place-and-route and binary file generation can be used.

Adding to the benefits, Barry Tso, regional manager, Avnet Electronics Marketing Asis, says "FPGA is a standard product and easily available off-the-shelf. With an extensive library of intellectual property (IP) available for use, you can change design in hours."

Prashant Aggarwal, vice president technology, Virtual Wire Technologies, comments. "The design and development cycle for an ASIC design is 2-3 years, while with FPGA it's few months to about a year." This helps in serving the constantly changing requirement of the market.

An FPGA, uses smaller wiring channels, for connecting logic blocks. A Logic blocks consists of smaller logic elements. A logic element has only one Flip Flop that is individually configured and controlled. Logic complexity of a logic element is only about 10 to 20 equivalent gates.

A further enhancement in the structure of FPGAS is the addition of memory blocks that can be configured as a general purpose RAM. An FPGA is an array of many logic blocks that are linked by Horizontal & Vertical wiring channels.

FPGA RAM blocks can also be used for logic Implementation or they can be configured to from memories of various word sizes and address space. Linking of logic blocks with the I/O cells and with the memories are lone through wiring channels. Within logic blocks, smaller logic elements are linked by local wires.

1.3 Description:

However, Pankaj Sathe, executive director and head of the Semiconductor Solutions Group, KPIT Cummins, provides a very practical perspective. He says "The trend towards lower geometries and faster transistors has somewhat slowed down. In an effort to keep place, parallel computing is evolving. It is expected that even embedded devices will have more than 60 microprocessor cores by 2015. And, since speed is no longer the main differentiator, improvement in manufacturing technologies are no longer sought after so much, as in the past. However, yield improvement technologies are gaining traction in the physical design space."

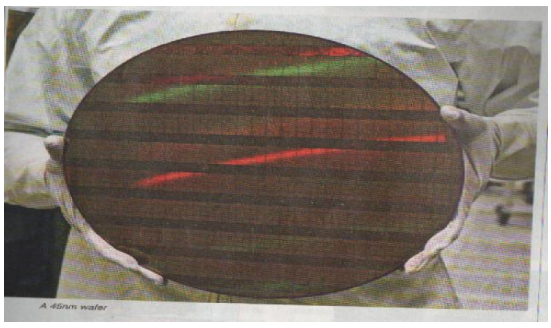

Figure: 3. Semiconductor Layer

This is not to be misconstrued as a reduction in the amount of innovation in the space. It is just that the goals are changing. Today, researchers are working to address immediate concerns such as yields

improvement, power management, cost and time-to-market, while also looking at futuristic options such as carbon nanotubes.

There have been significant developments in recent times. Listing some examples, professor Srikanth Jadcherla, chairman and CEO, Seer Akademi, says, "Kingston has developed what it claims to be the fastest Intel-certified memory in the world, which runs at 2400 MHz. Samsung has announced that it is now shipping 32GB NAND memory chips using 30nm technology, allowing to double the capacity of Samsung's previous generation. 45.72cum (18-inch) wafer prototypes are being talked about."

Sathe adds more examples such as the mainstream adoption of 40nm manufacturing technology that is helping some semiconductor sectors improve manufacturing margins and the adoption of the fab-lite model that is help in removing manufacturing volatility.

Let us take a look at some of these developments.

FPGAs aren't just the logic gates

The first FPGA from XC2064 had 64 configurable logic blocks and two 3-input look-up tables (LUTs). Today, we have FPGAs with millions of logic cells and many integrated blocks in a very tiny area. In the electronics industry, something that is programmable and switch able was always available in terms of discrete logic components, programmable logic devices (PLDs), etc.

"The whole idea was to replace or integrate the logic components (What we refer to as ghee logic) into a single component." As the silicon technology developed, the number of logic cells, capabilities and the speed of FPGAs increased.

When FPAGs were introduced, these were blank hardware chips. "With advancements in technology, FPGAs included more and more features on chip, like RAM and digital signal processing (DSP) blocks, memory controller, high-speed serial input / output transceiver and hard intellectual property (IP) for PCIE and Ethernet MAC," informs Tso. "Three is an extensive library of IP available to use and as the technology improve, there would be more and more features adding to it,"

1.4 Design & Implementation:

New challenges. At 32 nm and below, the intricate process and layout interactions cause failures that are not foreseen by normal simulation tools. Irregularity in logic also causes failures. The very low 'K' factors in lithography are also causing problems these days. At the 32, 28 and 22 nm levels, this leads to deigns sensitivities such as hot spots (areas on the die surface that exhibit excessive hearting).

Modeling and simulation. Everything including system-level power, gate oxides, etch transfers and line edge roughness has to be measured, modeled and simulated – nowadays even at the atomic level-to spot such problems. Some fabs monitor as many as 50,000 points. Of course, errors do not show up immediately by watching a single wafer. Sometimes, they are found only after monitoring hundreds or thousands of wafers. From fab to design and back. The key goal behind such modeling and monitoring is to immediately identify problems and their root cause, and correct them at the design stage. All metrology date from the fab has to be fed back to the design centers, and design improvements flown back. This is what most latest diagnostic tools such as those from Mentor Graphics and Synopsys attempt to do. From lithography, manufacturing process to object-oriented process control, everything has to be taken care of at the design stage. This is leading to adoption of many techniques like design based inspection and design-for-manufacturing (DFM). "DFM is one area where improvements are being made specifically in phase-shift-mask and OLE process control (OPC) techniques. However, exactly how they help in improving the yield is not clear," says Prof. Jadcherla.

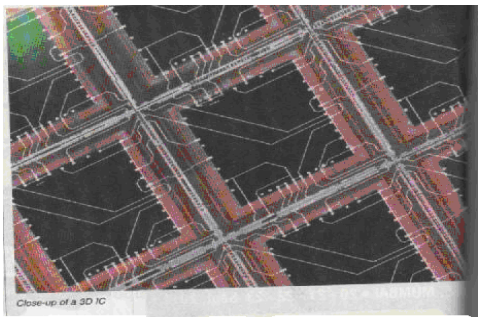

Figure: 4. Design by lithography

Identifying problems and improving the yield is no mean task and could take around a year to achieve even for the most experienced companies-as it happened during the introduction of the 40nm process at TSMC, the world's largest semiconductor manufacturer. When a new manufacturing process is introduced, it is first developed and refined in a test fab and then transferred to production lines in a process called 'chamber matching.' This theoretically ensures standard conformity and higher yields. Problems with chamber matching on TSMC's 40nm lines caused yield problems, thereby making it difficult for the company to match up to the demand for 40nm technology. It took almost a year for them to iron out these problems and plump up the yield of the process to match the previous generations.

1.5 Improvements in Lithography:

Lithography is one area in which a lot of improvements have been made, and are expected in the near future-especially due to the advancements made in photonics. As chips become smaller, there is an imminent move from 193 to 13.5nm-wavelength lithography in order to pattern finer features. This is due to pattern finer features. This is due to a new lithography technology called 'extreme-ultraviolet'

(EUV)(http://en.wikipedia.org/wiki/extreme_ultraviolet _lithography) which could allow current chip features to shrink by almost ten times. Since 2009, a variety of EUV tools have been launched, including EUV scanners for process development and EUV light sources.

Apparently, EUV requires a completely new yet cost-effective and reliable light source. Versions have been demonstrated that hit 100W output power, enough for minimal production. However, high-volume manufacturing will require double that figure. A recently launched EUV source from Cymer Inc. of San Diego uses a high powered infrared laser to bombard a microscopic molten tin droplet as much as 50,000 times per second. The resulting plasma radiates photons over a range of wavelengths. The 13.5nm light is collected and directed into the scanner illuminator. Japanese company Gigaphoton Inc. is also pursuing a similar laser-based approach. The company has announced plans to start shipping EUV light sources this year.

It is expected that by 2012, production systems for volume manufacturing using EUV lithography will be available. However, this is assuming that certain hurdles are mounted. Making masks of sufficiently high quality, for instance, is still a challenge. Another is checking for defects in those masks initially and after use. Companies such as KLA-Tencor Corporation and Carl Zeiss SMT are making mask inspection tools capable of handling 22nm logic node EUV masks. However these work using 193nm sources, and it is believed that they will work only up to 16nm process technology. So, what after that?

A review of the recently help SPIE Advanced Lithography – EUVl Conference by Vivek Bakshi (http://semimd.com/biog/2011/03/07/2011-spie advanced -lithography-%E2%80%93-euvl-conference-review/) provides an excellent overview of recent methods in lithography and metrology.

2. FPGAs with embedded DSP blocks:

Digital signal processing is required in every embedded application starting from audio – video devices to defense equipment. Any digital signal processing algorithm can be broken into the simplest architecture of multiply – and – accumulate function. Integrating these multipliers and accumulators on board with FPGAs serves a high – end alternative for DSP – intensive applications.

The natural question that arises is whether you can replace a DSP processor with an FPGA having a DSP block. The answer is both 'yes' and 'no'. "The difference between a DSP processor and a DSP – implemented FPGA is the same as between a software and a hardware. DSP is still a programmable processor and you write software programs that it runs," says Varma. He adds, "FPGA is a programmable hardware where everything runs concurrently. If you were to design a 256 – tap filter, in DSP you will have to run the filter 256 times as it runs the program sequentially. In FPGA, as it is hardware, the 256 – times run happens simultaneously in a single clock cycle". FPGAs are uniquely suitable for repetitive DSP tasks as they operate in parallel. However, dedicated DSPs are sometimes preferred because of their low cost in applications that do not demand repetitive and high performance.

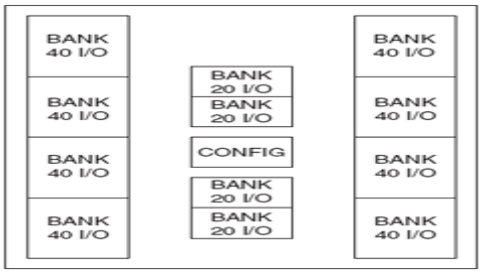

Figure: 5. CLB Details

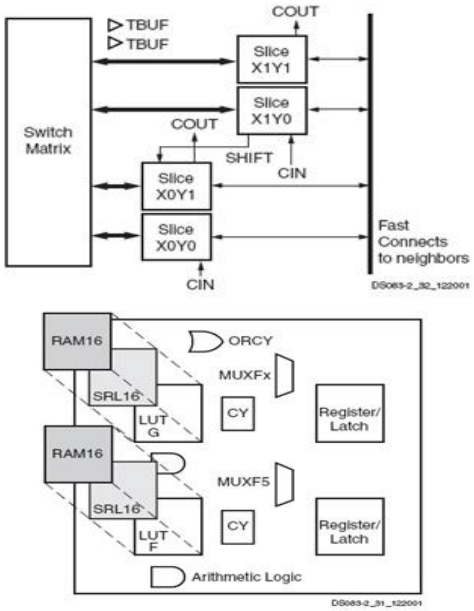

Figure: 6. FPGA hardware

Telecom technology is one of the early adopters of FPGAs for high – performance DSP applications. With the versatility if FPGAs, you are able to provide support for multiple platforms leading to a universal handset for different technologies (GSM, CDMA, 3G and 4G). FPGAs are also used in networking devices like wireless base stations, modems, switches and routers. "After evaluating the pros and cons of DSPs and FPGAs, we found that FPGAs are the most suitable for our multiple – input multiple – output (MIMO) system design. Our latest design of digital baseband for 4 x 4 MIMO system supports 180 MHz on FPGA with 60 percent utilization, which very good," With high – definition images and 3-D rolling, and growth in consumer electronics devices like the plasma TVs and digital cameras, there is a need for image processing algorithms that produce high – quality image. Image

processing operations are simple and repetitive, so these can best implemented using FPGAs with DSP block. But in image pipelining where 'blobs' and 'region of interest' in an object are inspected, a DSP may be preferred because of the varying sizes of blobs and subsequent processing required. There are certain scenarios where you will see a DSP and an FPGA being used together. Here, the algorithms are divided in computing – intensive tasks for FPGAs and others for the processor. This is called hard ware exploration.

Xilinx, Virtex – 5, Virtex – 6, Spartan – 6 and Extended Spartan – 3A, Acterl's RTAX, Altera;s Cyclone and Stratix and some of the FPGA families with embedded multiplier of varying bitlength used for digital signal processing applications.

3. High – Speed Serial I/O technology:

The data throughput requirements and chip – level functionality are increasing as high – speed communications start using FPGAs. This has compelled the industry to migrate form lower – data – rate parallel connections to higher – speed serial connections. This concept of Ser Des (serialiser – deserialiser) introduced by Lattice involves transmitting serialized date over high – speed, differential pairs rather than lower – speed parallel buses, facilitating higher data rates with fewer pins.

Shakeel Peera, director of marketing for high – density solutions, Lattice Semiconductors, shares, "There was an increasing need for low – cost FPGAs. However, these did not have high – speed interfaces. Through the concept of SerDes, we were abole to provide low-cost FPGAs with high-speed serial interface." SerDas serves a wide market, including wired and wireless communications (like microwave radio link), automotive, broadcasting video, industrial automation, printers and medical imaging application.

Serial standards and protocols like PCI express, serial rapid I/O and serial Bite are accepted in high-speed serial transceivers. " These high-speed serial transceivers supporting speed of up to 10.3125 Gbps 9also called 'multi-giga-bit transceivers') are now integrated in high-end FPGAs offering the benefits of less board space and increased flexibility and eliminating the interfacing issues for the board designers," shares Varma. High-speed serial solutions are applicable in next-generation telecommunication, networking and storage applications.

4.Fusion Mixed – Signal FPG as:

There is a common understanding that FPGAs are only digital devices. However, there are certain mixed-signal field-programmable analogue fabric and digital fabric. Such mixed-signal FPGAs find applications in power management, smart battery charging, clock generation and management, and motor control, which are still served by discrete analogue components, mixed-single ASICs or microcontroller units with embedded analogue-to-digital converters (ADCs). An MCU with embedded ADC has limitation on the number of analogue inputs and the speed at which it operates is relatively low.

Analogue control can be differentiated from digital control by a simple example of the dimming light application. Analogue signals process the output continuously as opposed to digital control of the dimming in steps. In short, real-world applications are more associated with the analogue domain, while digital comes in when you need to store and process the date.

The Fusion family form Actel is claimed to be the first embodiment of mixed-signal FPGAs. The architecture supports a 12-bit internal ADC at a sampling speed of 600 KB /s, eliminating the need for external mixed-signal support ICs. It can take 30 high-volt-age-tolerant analogue inputs. Fusion devices eliminate the need for multi voltage and power-up sequencers. These operate off a single 3.3V supply. The combination of single-voltage operation and power management makes them ideal for system/board management applications.

5. FPGAs With Embedded Processor Cores:

Inclusion of memory and other blocks on FPGAs have made them suitable for implementing the entire system-on-a-chip with in-built processor core. The advantage of implementing processor and its mix in the programmable logic fabric is the immense hardware-software flexibility. There are two approaches provided by major FPGA vendors for the embedded processor core. The hard-core processor has dedicated silicon on the FPGA chip, while you can implement soft-core entirely using the hardware descriptive language (HDL). As hard core is fixed on the chip, it does not provide the flexibility of soft cores.

The first processor core designed by ARM along with Actel specifically for implementation in FPGAs in 32-bit Cortex M1. The ARM cortex M1 development kit for Altera's Cyclone III FPGAs provides soft-core implementation. Xilinx' Microblaze, Altera's Nios II, and Lattice Mico 8 and Mico 32 are also soft-core implementations. The concept of multi-core processors and parallel computing can be extended to FPGAs in order to perform more complex embedded tasks.

6. Conclusion & Future work:

6.1 Changes Galore:

There are lot more trends catching up in the space. For example, device makers are moving towards a fab-lite model, whereby they handle only the designing and outsource the manufacturing to foundries, in order to avoid the cost of setting up a fab and the problems caused by changes in technology and demand.

Another trend is the focus on reducing the time-to-market. Since not much can be done to reduce the actual time of manufacture, the onus has shifted to the

design stage-more capable tools and processes are helping to reduce the time taken at this stage.

Sathe agrees, "The time taken for manufacturing and post-manufacturing process is generally fixed. Hence the emphasis is on reducing the design cycle time. An approach preferred these days in creating bigger system-on-chips is to reuse or but intellectual property, and to work with design partners rather than in-house development. The integrated device manufacturers are looking at a faster time-to-market and increasing market share rather than complete in-house design approach. New methodologies brought in by electronic design automation vendors, e.g., Magma's methodology to accelerate analogue porting and optimization, also help in this."

There is also an attempt to move from the current 30.5cm (12-inch) wafers to 45.7cm wafers. The 30.5cm, 300mm wafer-based technology, which itself is kind of new, yields 2.25 times more chips per wafer than the older 20.03cm (8-inch), 200mm wafers, yet they take just about the same time to pass through a factory, reducing the cost per chip and significantly boosting total monthly output. A 45.7cm wafer plant would show a similar reduction in per-chip cost and increase in output. However, as of now, nobody can afford a 45.7cm fab. An industry conglomeration, including TSMC, is looking at how to make 45.7cm fabrication more affordable. The company expects to bring it into operation by 2015. Let us wait and see what other changes happen by then.

6.2 New Concept: PSoC

Cypress Semiconductors has introduced a new concept of programmable system-on-a-chip (PSoC). Rajeev Mehtani, senior vice president, Cypress Semiconductor, explains, "PSoC devices encapsulate features of a microcontroller with flexibility and programmability of FPGAs and a configurable analogue sub-system." "Our chip comes with a sophisticated software that allows the users to program the digital and analogue sub-systems to their specific application, giving them ultimate control of the system design process," he adds.

6.3 Scope for improvement:

"FPGA as a technology has evolved, and has stated developing a lot of eco-system around it," says Rahul V. Shah, director, custom solutions, elnfochips. "The ecosystem means FPGA s with different features, different IP cores, tolls, evaluation board, reference de-sign from the vendors and designers.

FPGA vendors are providing newer FPGA chips with more and more functionality in sync with the market demand. However, in the race, the chips are not tested and verified thoroughly. "There is no chip which is bug-free" has now become applicable to FPGAs, which are coming with added complexities," says Shah. If the new chip is a derivative device, i.e., a variant of the already existing FPGA chip, it has the least probability of having a bug.

There are still certain application areas where ultra-low-power ASIC chips are preferred to FPGAs; e.g., in handheld devices. "FPGA technology has not reached a point so far where it will find its application in ultra-low-power devices. However, for a de handheld devices where performance is needed, such as the man-pack radio carried by soldiers for highly sophisticated wireless communication, FPGAs are preferred," shares Varma.

FPGAs sometimes show erratic behavior beyond certain temperature. "You cannot select an FPGA for your thermal requirement with just one parameter. You have to do a comparative study to determine whether the FPGA works fine at a particulars temperature or at a particulars frequency on a specific board," comments Shah. Aggarwal adds, "As long as you are working with the vendor's board, the specifications are well-mentioned. But for a custom-made board, these are not well documented. "The vendor documentation does of the required cooling fan, kind of cooling, temperature and even the weight of the fan- thinking that affect the device design.

Software tools for FPGA are still a problem for designers. Aggarwal says, "The tools are locked to a particular vendor and designers need to pay for the FPGA device as well as tools to the vendor." Prabhakar adds, "Every FPGA has its proprietary tool, so changing FPGAs in subsequent projects requires learning of a new design tool suite altogether. "There is a need for platform-independent tools for FPGA designers.

Despite technological advancement, FPGAs are still high on bill-of-material (BOM) price. "In most cases, the most expensive chop in a typical board BOM comes out to be an FPGA," says Prabhakar.

6.4 In a Nutshell:

FPGAs have moved from 130nm to 28nm process today. There is a lot of development and innovation happening to support additional features, programmability and flexibility. Also, the industry is extending support in terms of training the users on basic architecture, providing reference designs and helping them in custom designs.

"The bulk of the revenue for FPGAs comes from wireless and wired communications. This is the fastest growing segment across the globe. Display and security and surveillance are the other fast-growing applications based on FPGAs. These are the areas where we see India as a huge market," informs Peera.

"FPGAs are the best choice when volumes are of the order of a few hundred per annum. These are also the best choice while designing prototypes or proof-of-concept products as well as stepping stone towards ASIC design. All this is possible as FPGAs are

reprogrammable, field-upgradeable and easy to design. With all the new development, FPGAs are preferred in applications that are complex and performance-intensive," says Prabhakar.

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